



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,841	10/01/2003	Jae-Yong Jeong	4591-348	9906

20575 7590 12/22/2005

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER

LUU, MINER PHO

ART UNIT	PAPER NUMBER
----------	--------------

2824

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary

Application No.

10/677,841

Applicant(s)

JEONG ET AL.

Examiner

Pho M. Luu

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-31 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 17-31 is/are allowed.
- 6) ☒ Claim(s) 11 and 16 is/are rejected.
- 7) ☒ Claim(s) 12-15 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 09/21/05.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 21 September 2005 has been entered.
2. Claims 1-10 has been cancelled.
3. Claims 11-31 are pending in application.

Information Disclosure Statement

4. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 21 September 2005. The information disclosed therein was considered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Art Unit: 2824

6. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not explained how deactivating all the column selection signal and turning on selected ones of the column selection transistor in response to deactivating all the column selection signal by decoding a column address could be use in a stress test method for a flash memory device.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurlyama et al. (US. 5,559,744).

Regarding claim 11, Kurlyama et al. in Figure 4 discloses a stress test method (test signal TSI setting all of column selection transistor 28-1, 28-n into the column decoder 26-1, 26-n, see column 8, lines 45+) for a flash memory (EPROM, column 7, lines 21-22) device having column selection transistor (28-1, 28-n) configured to select a predetermined bit line (column decoders 26-1, 26-n are supplied to the gate of column selection transistor 28-1, 28-n which are connected to bit line BL1, BLn, see column 7,

lines 34-38) from among a plurality of bit lines that are coupled to flash memory cells, the stress test method comprising:

activating a plurality of column selection signals to a high voltage (column decoder 26-1, 26-n set at high voltage, see column 8, lines 19-23);

applying the plurality of column selection signals (column decoder 26-1, 26-n receive signal CA, CAn to generate output to selection transistor 28-1, 28-n) to all the column selection transistor (28-1 to 28-n). Regarding the function of deactivating all the column selection signals and turning on selected ones of the column selection transistors in response to deactivating all the column selection signals by decoding a column address is a normal operation, therefore, this limitation is inherently in the read and/or write normal operation of Kuriyama et al device.

With respected to claim 16. Kuriyama et al. in Fig. 4 disclosed that the column selection transistors are NMOS transistors (28-1 to 28-n).

Allowable Subject Matter

9. Claims 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record do not disclose or suggest a claims of the invention as recited in claims 12-15. In particular, the stress test method for a flash memory device wherein activating a plurality of column selection signal to a high voltage includes

providing the high voltage directly from an external source (claims 12-13) and applying a constant voltage to the plurality of bit lines (claim 14-15).

10. Claims 17-31 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to provide: **“level shifters configured to generate column selection signals that are applied to gates of the column selection transistors in response to an output of the decoder units wherein the level shifters are configured to apply a high voltage to all the column selection transistors during a stress test in response to the all column selection signal”** as claimed in the independent claim 17 and independent claim 24. The dependent claims 18-23 and 25-31 are also allowed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

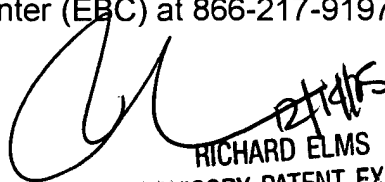
Atsumi (US. 5,243,569) disclosed a differential cell type eeprom incorporating stress test circuit for controlling in a stress test mode.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
December 8 2005


RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800